What is claimed is:

1. A ferroelectric memory cell for use in a ferroelectric random access memory (FeRAM) device, the ferroelectric memory cell comprising:

a first active area incorporating therein a gate of a depletion mode transistor;

a second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor;

a word line coupled to the gate of the depletion mode transistor and the gate of the enhancement mode transistor; and

a ferroelectric capacitor coupled to a drain of the enhancement mode transistor, for storing data.

2. The ferroelectric memory cell as recited in claim 1, wherein the first active area of the memory cell is coupled to first active areas of neighboring memory cells, thereby forming a bit line.

3. The ferroelectric memory cell as recited in claim 2, wherein the bit line is parallel with a cell plate line of the ferroelectric capacitor.

4. The ferroelectric memory cell as recited in claim 1, wherein the first and the second active areas are n-types.

5. A ferroelectric random access memory (FeRAM) device including a plurality of ferroelectric memory cells, comprising:

first active areas incorporating therein gates of depletion

mode transistors;

second active areas adjacent to the first active areas incorporating therein gates of enhancement mode transistors;

word lines coupled to the gates of the depletion mode transistors and the gates of the enhancement mode transistors; and

ferroelectric capacitors coupled to drains of the enhancement mode transistors, for storing data.

6. The ferroelectric memory device as recited in claim 5, wherein said first active areas are coupled to each other, thereby forming a bit line.

7. The ferroelectric memory device as recited in claim 6, wherein the bit line is parallel with a cell plate line of the ferroelectric capacitors.

8. The ferroelectric memory device as recited in claim 5, wherein the first and the second active areas are n-types.

9. The ferroelectric memory device as recited in claim 6, further comprising a sense amplifier for sensing and amplifying data applied to the bit line to generate an amplified signal.